IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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M. Rodgers

In re. Application of:	**CSONKA, Jacqueline V., and CHONG, Ignatius T.**
Filed:	**December 19, 2000** **Date: December 19, 2000**
Title:	**TRACE-PAD INTERFACE FOR IMPROVED SIGNAL QUALITY**
Atty's Docket No.:	**51636/142**

United States Department of Commerce
Patent and Trademark Office
Commissioner of Patents and Trademarks
Washington, D.C., 20231
U.S.A.

PRELIMINARY AMENDMENT

This is a Preliminary Amendment to the enclosed application. Please amend the application as follows in view of the comments set out below:

IN THE SPECIFICATION:

On page 1, line 10, after "components" add --, such as component 7 in Fig. 1A--.

On page 1, line 11, after "pinouts or leads" add -- 5--.

On page 1, line 11, after "printed wire board" add -- 14--.

On page 1, lines 11-12, after "pin or lead" add -- 5--.

On page 1, line 12, after "electronic component" add -- 7--.

On page 1, line 13, after "pad" add -- 12--.

On page 1, line 13, after "printed wire board" add -- 14--.

On page 1, line 15, after "component pads" add -- 12--.

On page 1, line 17, after "printed wiring board" add -- 14--.

On page 1, line 17, after "traces" add -- 10--.

On page 2, line 3, replace "As" with --Referring to Fig. 1B, as--.

On page 2, line 4, after "digital signals" add -- 17--.

On page 2, line 5, after "printed circuit board" add -- 14--.

On page 2, line 5, after "various components" add – 7 and 7a--.

On page 2, line 6, after "destinations" add -- 7a--.

On page 2, line 6, after "input receivers" add -- 19--.

On page 2, line 7, after "example" add --, as shown in Fig. 1C--.

On page 2, line 8, after "control signals" add -- 42--.

On page 2, line 8, after "memory controller" add -- 40--.

On page 2, line 9, after "the memory" add -- 64--.

On page 6, after the description of Fig. 1 on lines 8-9, insert the following lines:

--Fig. 1A is a schematic diagram of a component on a printed circuit board as is in the prior art; --

--Fig. 1B is a block diagram of two components connected on a printed circuit board; --

--Fig. 1C is a block diagram of a memory controller and memory as an example of two components connected on a printed circuit board; --

On page 10, line 15, after "another circuit board" add --43. The DIMM printed circuit board 43 connects to slot 48 via an edge connector 45--.

On page 10, line 20, after "DIMM memory" add --47--.

On page 11, line 1, after "printed wire board" add --43--.

On page 11, line 1, after "signal traces" add --22--.

On page 11, line 2, after "control signals" add --42--.

On page 11, line 2, after "corners of the pads" add --24--.

On page 11, line 4, after "DIMM memory" add --47--.

On page 11, line 5, after "DIMM printed circuit board" add --43--.

On page 11, after line 6, insert new paragraph

--Referring to Fig. 8, the edge connector 45 attaches the DIMM printed circuit board to the printed circuit board containing the memory controller. The DIMM memory components attach to the DIMM printed circuit board. As can be seen from Fig. 8, areas 80-87 have the connect structure of the pads with the traces as described in the invention and as shown in Fig. 4.--

IN THE CLAIMS:

Cancel existing Claims 1-11 inclusively. Replace the cancelled claims with the following new Claims 12-36.

Claim 12 (new). The apparatus for a signal-triggered digital circuit, said apparatus comprising:

a signal source for generating a digital signal;

an input receiver, said input receiver receiving said digital signal for said digital circuit and being responsive to triggering induced by said digital signal;

a conducting interface;

a conducting signal path, said conducting signal path being electrically connected to said conducting interface, said conducting interface being electrically connected to said input receiver, said signal path carrying said digital signal thereover; and

wherein said conducting interface is substantially rectangular in planar view and said conducting signal path connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of said conducting interface to which said conducting signal path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees.

Claim 13 (new). The apparatus according to Claim 12, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

Claim 14 (new). The apparatus according to Claim 13, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of the said digital signal is selected from a group comprising a rise time thereof and a fall time thereof.

Claim 15 (new). The apparatus according to Claim 14, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

Claim 16 (new). The apparatus according to Claim 13, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

Claim 17 (new). The apparatus according to Claim 16, further comprising a circuit substrate, wherein said input receiver and said conducting interface are located on said circuit substrate.

Claim 18 (new). The apparatus according to Claim 17, wherein said circuit substrate comprises a printed circuit board and wherein said conducting interface is a pad and said conducting signal path is a trace.

Claim 19 (new). The apparatus according to Claim 18, wherein said pad is substantially square in planar view.

Claim 20 (new). The apparatus according to Claim 18, wherein said trace has a width which is 1/5th of a width of said pad to which said trace is connected.

Claim 21 (new). The apparatus according to Claim 18, wherein when said input receiver is mounted to said pad, said trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of said pad to which said trace is connected.

Claim 22 (new). The apparatus according to Claim 18, wherein when said input receiver is mounted to said pad, said pad has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said trace has a width of 4 mils and a thickness of 1.2 mils.

Claim 23 (new). The apparatus according to Claim 18, wherein the apparatus is a memory system which further comprises a memory device, wherein said signal source is a memory controller which generates digital signals in the form of control signals carried by said trace, and wherein said input receiver is located within said memory device.

Claim 24 (new). The apparatus according to Claim 23, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

Claim 25 (new). The circuit substrate for a signal-triggered digital circuit, said circuit substrate comprising:

a conducting interface, substantially rectangular in planar view, for electrical connection to an input receiver, said input receiver receiving a digital signal over said digital circuit and being responsive to triggering induced by said digital signal;

a conducting signal path having a width which is 1/5th of a width of said conducting interface, said conducting signal path being connected to said conducting interface, said signal path carrying said digital signal thereover; and

wherein said conducting path connected to said conducting interface has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of the conducting interface to which said path is connected to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting path when compared to a connection wherein said angle has a value of 90 degrees.

Claim 26 (new). The circuit substrate according to Claim 25, wherein said conducting interface is substantially square in planar view.

Claim 27 (new). The circuit substrate according to Claim 25, wherein said conducting signal path has a thickness which is in a range of 1/5th to 1/6th of a thickness of the conducting interface to which said conducting signal path is connected.

Claim 28 (new). The circuit substrate according to Claim 25, wherein when said input receiver is mounted to said conducting interface, said conducting interface has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein said conducting signal path has a width of 4 mils and a thickness of 1.2 mils.

Claim 29 (new). The circuit substrate according to Claim 25, wherein said conducting signal path is connected to the conducting interface at a corner thereof.

Claim 30 (new). The circuit substrate according to Claim 29, wherein said conducting signal path has a length which is at least 1/6th of a transition electrical length of said digital

signal carried thereover, said transition electrical length constituting a transient time of said digital signal multiplied by a propagation speed of said digital signal over said conducting signal path, and wherein said transient time of said digital signal is selected from a group comprising a rise time thereof and a fall time thereof.

Claim 31 (new). The circuit substrate according to Claim 30, wherein said conducting signal path has a length which is at least said transition electrical length of said digital signal carried thereover.

Claim 32 (new). The circuit substrate according to Claim 29, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

Claim 33 (new). The circuit substrate according to Claim 32, wherein said circuit substrate comprises a printed circuit board, said conducting interface is a pad and said conducting signal path is a trace.

Claim 34 (new). The circuit substrate according to Claim 33, said circuit substrate further comprising an input receiver and a signal source for generating said digital signal.

Claim 35 (new). The circuit substrate according to claim 34, said circuit substrate further comprising a memory device, wherein said signal source is a memory controller which generates digital signals in the form of control signals carried by said trace, and wherein said input receiver is located within said memory device.

Claim 36 (new). The circuit substrate according to Claim 35, wherein said circuit substrate further comprises a slot and wherein said memory system further comprises a memory module on which said memory device is located, said memory module being a dual in-line memory module (DIMM) comprising an edge connector, said DIMM being connected to said memory controller by said edge connector connecting to said slot.

IN THE DRAWINGS:

It is requested that the two sheets of drawings containing Figures 7 and 8 be cancelled and replaced with the enclosed substitute sheets, for which duplicates have been submitted to show the proposed drawing changes in red. Three additional sheets have been provided for Figures 1A, 1B, and 1C, respectively.

REMARKS

Applicants have amended the specification and claims in order to comply with the Examiner's objections as set out in the Office Action dated June 19, 2000 in parent application serial no. 08/951,556.

The specification of the present continuation application reflects the language of the parent application, as originally filed, together with all amendments of record thereto which had not been objected to by the Examiner.

Figure 1A has been added. It shows a schematic diagram of the prior art. This is a diagram of a component 7 with multiple leads 5 on a printed circuit board 14. It shows a component 7 with multiple leads 5 connected to a pad 12 on the printed circuit board 14 as

described on page 1, lines 8-11. The pads are connected to traces 10 at 90° angles as is described on lines 13-19.

Figure 1B has been added. It shows a block diagram of two components, 7 and 7a, connected on a printed circuit board 14. The components are connected via a trace 10 as is described on page 1, lines 13-15. Digital signals 17 travel from component 7 to component 7a on printed circuit board 14 as is described on page 2, lines 2-4. The destination component 7a has an input receiver 19 which is triggered by the digital signal 17 as is described on page 2, line 4.

Figure 1C has been added. It shows a block diagram of a memory controller and memory as an example of two components connected on a printed circuit board. On page 2, lines 5-7, the memory controller and the memory are described as an example of the description on page 2, lines 1-5. Therefore, the diagram of Figure 1C is almost identical to that of Figure 1B, the diagram depicting the description of page 2, lines 1-5. Figure 1C has component 7 replaced by memory controller 40, digital signal 17 replaced by control signal 42, and component 7a replaced by memory 64. This is in accordance with the specific example described on page 2, lines 5-7.

The Figures 1A, 1B, and 1C and their descriptions are illustrations of the explanations provided on pages 1-2 of the application. As such, no new matter has been added by adding these figures, their descriptions, and reference numbers to the drawings on pages 1-2.

In Figure 7, a number of elements have been added. One such element is DIMM printed circuit board 43. The DIMM printed circuit board 43 is described on page 10, lines 14-15 as a separate printed circuit board where the DRAM DIMMs reside. DIMM printed circuit board 43 connects to slot 48 via an edge connector 45. The edge connector 45 was shown but previously unlabelled in Fig. 8. The edge connector is now labelled in Fig. 8 and is shown in Fig. 7. The

description on page 10, lines 13-14 shows how the DIMM is connected to DIMM slot 48. This has now been illustrated in Fig. 7 and described on page 10 after line 15. Another new element in Fig. 7 is DIMM memory 47 which resides on the DIMM printed circuit board 43. This is described on page 10, lines 14-15 and also lines 17-20 stating that the DIMM printed circuit board 43 is a separate printed circuit board than that containing the memory controller and that the DIMM memory 47 is contained on the DIMM printed circuit board 43. Combining Fig. 1C with the memory as described on page 10, lines 17-20 gives memory, in this case DIMM memory 47, with an input receiver 19, connected to memory controller 40 which sends control signals 42 to DIMM memory 47 via a trace. This has been illustrated in Fig. 7 in accordance with the description on pages 2 (as per Fig. 1C) and 10. As such, no new matter has been added with the amendment to Fig. 7.

Fig. 8 has had reference numerals added to it. The drawing had been previously described on page 11, lines 4-6 as a DIMM printed circuit board made in the manner as described in the specification. As stated previously, the edge connector that was previously shown in Fig. 8 has now been identified by means of a reference numeral. The definition of a dual-in-line memory module (DIMM) was downloaded from *IT Windows Library*, produced by Penton Media Inc., http://windowsitlibrary.com/Content/175/02/7.html on December 12, 2000. A copy of this website is attached. It defines a DIMM as a "RAM package that holds several memory chips on a single circuit board and has a 168-pin single-row edge connector for insertion into the motherboard". An edge connector is an inherent part of a DIMM and was shown in the original Figure 8. The existence of a memory chip or component attached to the printed circuit board is also inherent in the structure of the DIMM. Areas 80-87 that can be seen to have the structure of the invention as is shown in Figure 4 have been marked. An explanation of this has been added

on page 11. As this is an explanation of the definition and inherent structure of the DIMM, this is not new matter.

The drawings have been changed from the present application to comply with the Examiner's objections on page 2 of the Office Action. The Preliminary Amendment provides that every feature of the invention is shown in the drawings and a description of how Figure 4 relates to Figure 8 has been added as per the drawing objection found at subparagraph 1 of paragraph 1 on page 2 of the Office Action. Please note that subparagraph 2 of the drawing objections has been corrected in the present application by cross hatching Figure 4A. Also, subparagraph 3 of the drawing objections has been corrected in the present application by drawing the angle theta (θ) as between the longitudinal centerline axis of the trace and a side of the pad, as is described on page 7, lines 16-20 of the specification.

The Examiner's objection in the first paragraph of page 3 has been addressed in the present application. Please note that on page 7, line 19 that the angle theta (θ) has been described as being located between the longitudinal centerline axis of the trace and proximate side 26b of the pad, as is shown in Figure 4.

The Examiner had objected to Claims 16-26 of the parent application. These claims exist in the continuation application as Claims 1-11. The existing Claims 1-11 in the continuation application have now been cancelled and replaced with new Claims 12-36.

The Examiner had rejected Claims 18 and 19 of the parent application (existing Claims 3 and 4) under 35 U.S.C. 112, first paragraph, in paragraph 5 and 6 of the claims objections on pages 3-4 of the Office Action. The Examiner had been of the view that these claims contained subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s) at the time the application was filed, had possession of the claimed invention. The Examiner had contended that the "transition electrical length" as defined in Claim 18 of the parent application (existing Claim 3) was not supported by the specification and that the length of the signal and transient time were not disclosed.

Claim 18 of the parent application (existing Claim 3) has been cancelled and now appears as new Claim 14. Claim 19 of the parent application (existing Claim 4) now appears as new Claim 15. The claim element recited in new Claim 14 is the "transition electrical length" and not "transitional electrical length" as was previously recited. It is respectfully submitted to the Examiner that "transition electrical length" as it was found in Claim 18 of the parent application (existing Claim 3) is found in the specification on page 8, lines 13-17. Although the Examiner has taken the position that the term "transition electrical length" is not adequately described in the specification of the parent application, as it can be seen in the reference attached, Lee Ritchey, "High Speed PCB Design" (Presented at PCB Design Conference, March 20, 1995), at page 4, that "transition electrical length" is a term known in the art. The more common name for this term is the "effective length of the electrical feature", as can be seen in the reference attached, Johnson, Howard & Graham, Martin, *High-Speed Digital Design* (New Jersey: Prentice Hall, 1993) at page 7. The electrical feature that is discussed in this application is the rise or fall, i.e. the transition, of the digital signal, as described on page 8, lines 15-16 of the present specification. As such, the topic addressed on the said page 8 is the effective length of the transition or transition electrical length. Please note that the propagation speed along a signal trace is the inverse of the propagation delay of the signal. This gives the formula on page 7 of *High-Speed Digital Design* as being equal to the formula on page 8, lines 14-16.

It is respectfully submitted to the Examiner that there is no mention of the length of the signal in Claim 18 of the parent application (existing Claim 3). Perhaps the Examiner meant the transition electrical length of the signal. If so, the transition electrical length, as stated previously, is presented in the current specification on page 8, lines 13-17 as well as being a term known in the art.

The Examiner also had objected to Claims 18 and 19 of the parent application (existing Claims 3 and 4) because the transient time was not disclosed. It is respectfully submitted that the transient time is a generic expression for denoting either the rise time or the fall time. Transient time is merely an expression that encompasses both events. The reason for encompassing both events is shown on page 8, lines 13-17 of the specification where the transition electrical length is defined as either the rise time or the fall time multiplied by the propagation speed. As can be seen in the attached reference Johnson, Howard & Graham, Martin, *High-Speed Digital Design* (New Jersey: Prentice Hall, 1993) at page 7, it is well known in the art that it is the fastest electrical feature that is the significant feature.

No change was made to new Claims 14 and 15 from Claims 18 and 19 of the parent application (existing Claims 3 and 4) other than that listed above i.e. "transitional" changed to "transition". As such, no new matter has been added with these claims.

The Examiner had rejected Claim 16 of the parent application (existing Claim 1) under 35 U.S.C. 112, second paragraph, in paragraph 5 of the claims objections on page 4 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regarded as the invention. Specifically, the Examiner had stated that "associated with" is indefinite. Claim 16 of the parent application (existing Claim 1) has been cancelled and rewritten as new Claim 12. This wording has been removed in new Claim 12.

The Examiner also had stated that Claim 16 of the parent application (existing Claim 1) is indefinite because the signal source and signal receiver are not claimed. New Claim 12 explicitly claims the signal source and the input receiver. Both the signal source and the input receiver are mentioned on page 2 of the current specification. The input receiver is mentioned on lines 6 and 14 as part of the destination component for the digital signal. On page 2 at lines 4-7, the description speaks of digital signals that travel along a trace between components and reach a destination. The source component is therefore inferable from this phrase since the source component generates the digital signal which is sent to the destination component. As such, no new matter has been added by new Claim 12 by explicitly claiming the signal source and input receiver.

Since new Claim 12 now explicitly recites the input receiver, this will address the Examiner's objection to Claim 24 of the parent application (existing Claim 9) in the first paragraph on page 5 of the Office Action.

The Examiner had objected to Claims 25 and 26 of the parent application (existing Claims 10 and 11) as being indefinite because the elements recited were not part of the circuit substrate claimed in Claim 16 of the parent application (existing Claim 1). The element of the memory module from Claim 25 of the parent application (existing Claim 10) has now been explicitly claimed in new Claim 23 of the present application as a memory device. A specific example of the memory device is recited on page 2, lines 7-9 as "memory". As can be seen with Figure 1C, the input receiver is located within the memory, as is recited in new Claim 23 of the present application. As such, no new matter has been added.

The elements of the edge connector and the slot are now explicitly claimed in new Claim 24 which corresponds to Claim 26 of the parent application (existing Claim 11). The slot

appears in the present specification on page 10, lines 13-14. The edge connector was previously present but unlabelled in Figure 8. The DIMM, according to the claim, is attached to the slot as in the manner described on page 10, lines 13-14. As such, no new matter has been added by explicitly claiming these elements.

Claim 17 of the parent application (existing Claim 2) has been cancelled and rewritten as new Claim 13. Claim 20 of the parent application (existing Claim 5) has been cancelled and rewritten as new Claim 16. Claim 23 of the parent application (existing Claim 8) has been cancelled and rewritten as new Claim 21. Claim 24 of the parent application (existing Claim 9) has been cancelled and rewritten as new Claim 22. As such, no new matter has been added in new Claims 13, 16, 21 and 22.

Claim 22 of the parent application (existing Claim 7) has been cancelled and rewritten as new Claims 19 and 20. New Claim 19 does not include the limitation that the conducting interface be substantially square. This limitation is now recited in new Claim 20. As such, no new matter has been added.

Claim 21 of the parent application (existing Claim 6) has been cancelled and rewritten as new Claim 18. The difference between these claims is that the claim now states that the circuit substrate "comprises" a printed circuit board instead of "is" a printed circuit board. This is to comply with the description in the present specification on page 10, lines 14-15 where the substrate comprises more than one printed circuit board.

New Claim 17 has no counterpart in the old application. It introduces the circuit substrate that was recited in old Claims 16-26. As such, no new matter has been added with this claim.

On page 7, paragraph 8 of the Office Action, the Examiner stated that Claims 22-24 would be allowable if rewritten in independent form and to overcome all of the s. 112 rejections. Claim 22 of the parent application (existing Claim 7) has been rewritten in independent form as new Claim 25 as was suggested by the Examiner. New Claim 25 does not include the limitation that the conducting interface be substantially square. This limitation has been recited in new dependent Claim 26. Claims 23 and 24 of the parent application (existing Claims 8 and 9) have also been rewritten as new Claims 27 and 28 dependent on new Claim 25. As such, no new matter has been added with these claims.

New Claim 29 recites the same elements as were recited in Claim 17 of the parent application (existing Claim 2). New Claim 30 recites the same elements as were recited in Claim 18 of the parent application (existing Claim 3). New Claim 31 recites the same elements as were recited in Claim 19 of the parent application (existing Claim 4). New Claim 32 recites the same elements as were recited in Claim 20 of the parent application (existing Claim 5). New Claim 35 recites the same elements as were recited in Claim 25 of the parent application (existing Claim 10). New Claim 36 recites the same elements as were recited in Claim 26 of the parent application (existing Claim 11). As such, no new matter has been added with these claims.

New Claim 33 recites the same elements as were recited in Claim 21 of the parent application (existing Claim 6). The difference between these claims is that the claim now states that the circuit substrate "comprises" a printed circuit board instead of "is" a printed circuit board. This is to comply with the description in the specification on page 10, lines 14-15 where the substrate comprises more than one printed circuit board.

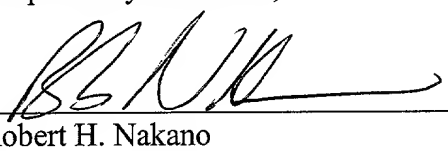
New Claim 34 has no counterpart in the old application. New Claim 34 explicitly claims the input receiver and signal source as is described in the above explanation of new Claim 12. For the same reasons as those stated above, this claim adds no new matter.

New Claims 12, 13, 14, 15 and 18 recite a digital signal source and input receiver. The Examiner had objected to Claims 16-19 and 21 of the parent application (existing Claims 1-4 and 6) as being anticipated by Merriman (U.S. 5,379,189). It is respectfully submitted that these objections will be avoided by the corresponding new Claims 12, 13, 14, 15 and 18. Additionally, it is respectfully submitted that these objections will be avoided in new Claims 25, 29, 30, 31 and 33 which recite the same elements as Claims 16-19 and 21 of the parent application (existing Claims 1-4 and 6). In new Claims 25, 29, 30, 31 and 33, the proportions of the path to the interface have been claimed as was suggested by the examiner on page 7, paragraph 8 of the Office Action.

New Claims 12 and 16 recite a digital signal source and input receiver. The Examiner had objected to Claims 16 and 20 of the parent application (existing Claims 1 and 5) as being anticipated by Campi (U.S. 4,485,362). It is respectfully submitted that these objections will also be avoided by the corresponding new Claims 12 and 16. Additionally, it is respectfully submitted that these objections will be avoided in new Claims 25 and 32 which recite the same elements as Claims 16 and 20 of the parent application (existing Claims 1 and 5). In new Claims 25 and 32, the proportions of the path to the interface have been claimed as was suggested by the examiner on page 7, paragraph 8 of the Office Action.

Entry of the present Preliminary Amendment is believed to be in order and such action in due course is earnestly solicited. The Examiner is invited to contact the undersigned by telephone to discuss this case further, if necessary.

Respectfully submitted,



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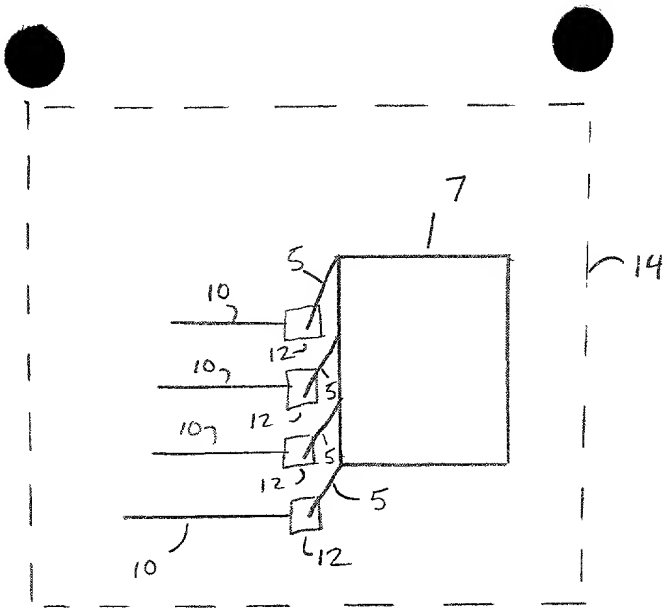

Fig 1A Prior Art

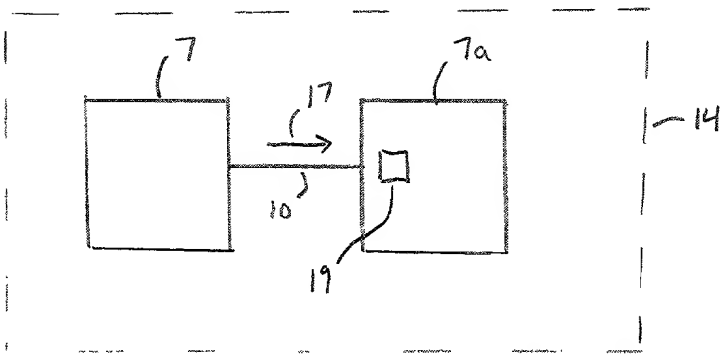

Fig 1B

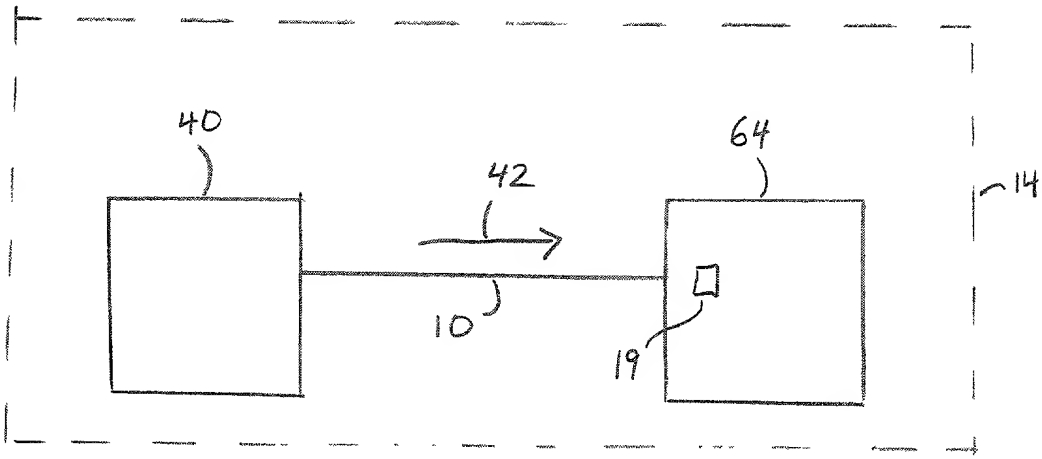

Fig 1C

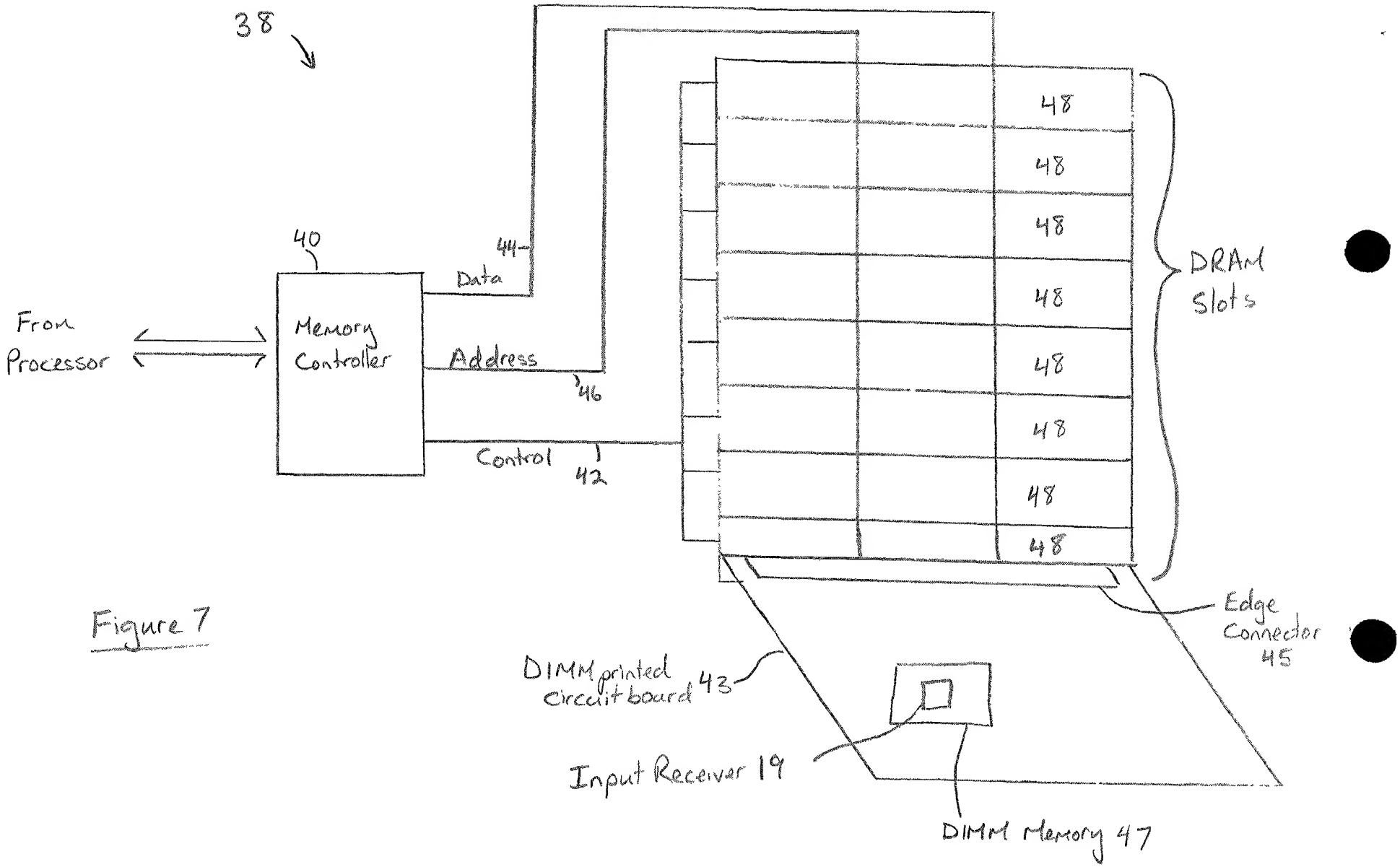
38
40
44
Data
Address
46
Control
42
From Processor
Memory Controller
48
48
48
48
48
48
48
48
DRAM Slots
Edge Connector 45
DIMM printed circuit board 43
Input Receiver 19
DIMM Memory 47

Figure 7

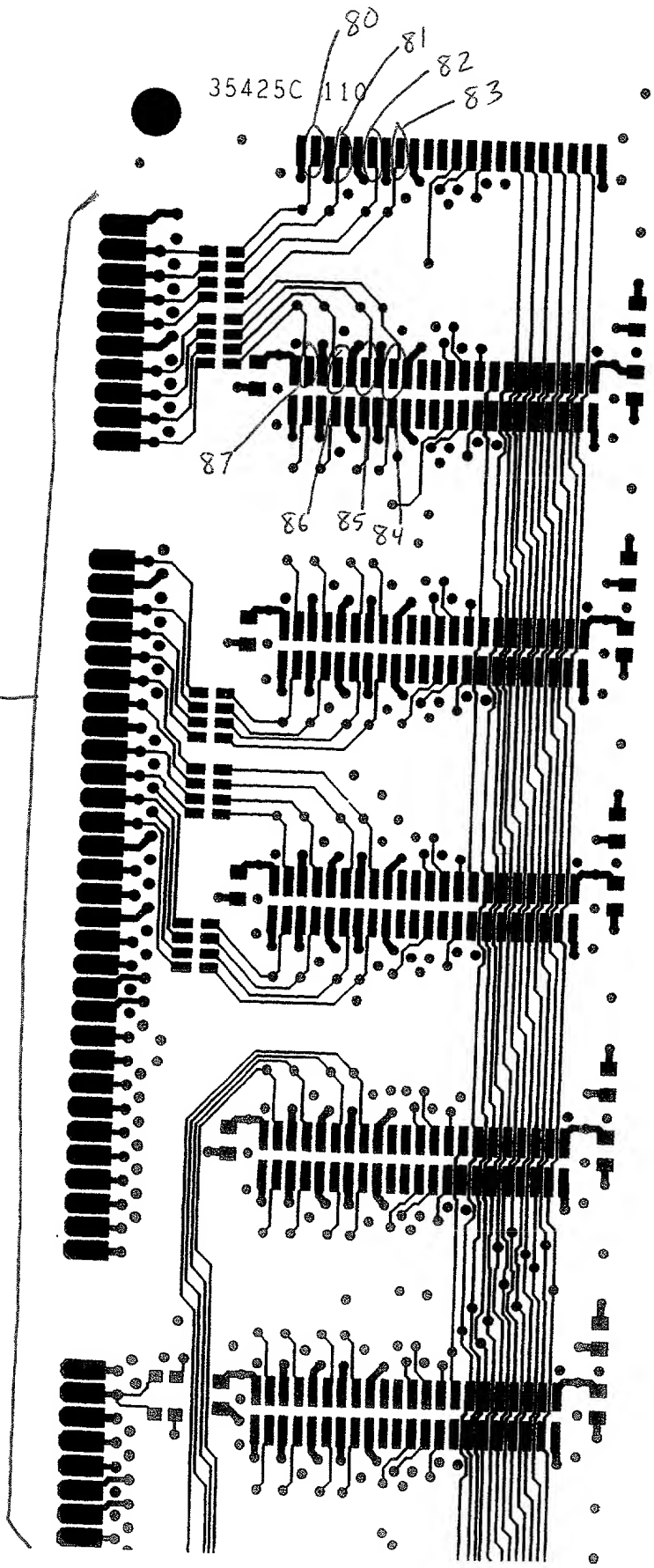

FIG. 8